VLSI TOPICS

SOFTRONIICS

AN ISO 9001:2015 Certified Company

CALICUT || PALAKKAD || COIMBATORE

WWW.SOFTRONIICS.IN

9037291113, 9995970405

Sl.No:	TITLE OF PAPER	YEAR OF PUBLISHING	CATEGORY OF PAPER
1	A 0.325 V, 600-kHz, 40-nm 72-kb 9T Sub threshold SRAM with Aligned Boosted Write Word line and Negative Write Bit line Write-Assist	2014	IEEE
2	A High Speed 256-Bit Carry Look Ahead Adder Design Using 22nm Strained Silicon Technology	2015	IEEE
3	A Highly-Scalable Analog Equalizer Using a Tunable and Current-Reusable Active Inductor for 10-Gb/s I/O Links	2014	IEEE
4	Convenience probe: a phone-based system for retail trade-area analysis	2014	IEEE
5	Smart home system using android mobile	2013	JOURNAL
6	Water level monitoring and control using smart phone	2013	JOURNAL
7	Global Built-In Self-Repair for 3D Memories with Redundancy Sharing and Parallel Testing	2013	IEEE
8	High-Speed and Energy-Efficient Carry Skip Adder Operating Under a Wide Range of Supply Voltage Levels	2015	IEEE
9	Voltage Mode Implementation of Highly Accurate Analog Multiplier Circuit	2015	IEEE
10	A Novel Realization of Reversible LFSR for its Application in Cryptography	2015	IEEE
11	Drowsy Driver Detection using Representation Learning	2015	IEEE
12	Medical Image Segmentation Using Edge feature based XILINX System Generator	2015	IEEE
13	GFCG: Glitch Free Combinational Clock Gating Approach in Nanometer VLSI Circuits	2015	IEEE
14	Low Power Compressor Based MAC Architecture for DSP Applications	2015	IEEE
15	Low Power Multiplier Architectures Using Vedic	2015	IEEE

	Mathematics in 45nm Technology for High Speed Computing		
16	Low-Cost Multiple Bit Upset Correction in SRAM-Based FPGA Configuration Frames	2015	IEEE
17	Power Optimization of Communication System Using Clock Gating Technique	2015	IEEE
18	Low-Power Programmable PRPG With Test Compression Capabilities	2015	IEEE
19	Voltage Mode Implementation of Highly Accurate Analog Multiplier Circuit	2015	IEEE
20	Low Power Multiplier Architectures Using Vedic Mathematics in 45nm Technology for High Speed Computing	2015	IEEE
21	Digital to Time Converter Using SET in HSPICE	2015	JOURNAL
22	Design of high speed ternary full adder and three input XOR circuits using CNTFETs	2015	IEEE
24	Design Method of Single-Flux-Quantum Logic Circuits Using Dynamically Reconfigurable Logic Gates	2015	IEEE
25	Design and Simulation of Single Layered Logic Generator Block using Quantum Dot Cellular Automata	2015	IEEE
26	Energy-Efficient Approximate Multiplication for Digital Signal Processing and Classification Applications	2014	IEEE
27	FPGA Implementation of Scalable Micro programmed FIR Filter Architectures using Wallace Tree and Vedic Multipliers	2015	IEEE
28	FPGA Implementation of Vedic Floating Point Multiplier	2015	IEEE
29	Aging-Aware Reliable Multiplier Design With Adaptive Hold Logic	2015	IEEE
		2015	IEEE

30	Design of Area and Power Efficient Digital FIR Filter Using Modified MAC Unit		
31	Design of Low Power and High Speed Carry Select Adder Using Brent Kung Adder	2015	IEEE
32	Design and Performance Evaluation of A Low Transistor Ternary CNTFET SRAM Cell	2015	IEEE
33	A 0.25-V 28-nW 58-dB Dynamic Range Asynchronous Delta Sigma Modulator in 130-nm Digital CMOS Process	2015	IEEE
34	A CMOS PWM Transceiver Using Self-Referenced Edge Detection	2015	IEEE
35	Read Performance: The Newest Barrier in Scaled STT-RAM	2014	IEEE
36	On the Non volatile Performance of Flip-Flop/SRAM Cells With a Single MTJ	2014	IEEE
37	High-Performance and High-Yield 5 nm Underlapped FinFET SRAM Design using P-type Access Transistors	2015	IEEE
38	Fully Reused VLSI Architecture of FM0/Manchester Encoding Using SOLS Technique for DSRC Applications	2014	IEEE
39	FPGA Implementation of an Advanced Encoding and Decoding Architecture of Polar Codes	2015	IEEE
40	A Novel VHDL Implementation of UART with Single Error Correction and Double Error Detection Capability	2015	JOURNAL
41	A Combined SDC-SDF Architecture for Normal I/O Pipelined Radix-2 FFT	2015	IEEE
42	A High-Performance FIR Filter Architecture for Fixed and Reconfigurable Applications	2015	IEEE
43	An Efficient VLSI Architecture of a Reconfigurable Pulse-	2015	IEEE

	Shaping FIR Interpolation Filter for Multi standard DUC		
44	**A Class of SEC-DED-DAEC Codes Derived From Orthogonal Latin Square Codes**	**2014**	**IEEE**
45	**A High-Throughput VLSI Architecture for Hard and Soft SC-FDMA MIMO Detectors**	**2015**	**IEEE**
46	**VLSI-Assisted Non rigid Registration Using Modified Demons Algorithm**	**2015**	**IEEE**
47	**A novel approach to realize Built-in-self-test(BIST) enabled UART using VHDL**	**2015**	**JOURNAL**
48	**DTMF Controlled Robot without Microcontroller**	**2015**	**IEEE**
49	**A Sub-mW, Ultra-Low-Voltage, Wideband Low-Noise Amplifier Design Technique**	**2014**	**IEEE**